

Abstract of the Disclosure:

A pipeline containing a fetch stage, a decode stage, an execute stage, and a write back stage is used for executing a method that provides a higher level of security to a CPU. The 5 write back stage contains at least one register whose use does not result in any state change of the CPU, and at least one register whose use does result in a state change of the CPU. At least one randomly selected code sequence is inserted in the decode stage as a placeholder code or dummy code sequence, 10 making an attack by DPA more difficult.

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